CEA-Leti and Silvaco Team Up on Yield-Prediction Project For Ultra-Low-Power Static Memories

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Project Combines CEA-Leti's Semiconductor Development Expertise and Silvaco's SPICE Simulation and Variability Analysis Technologies

LAS VEGAS – June 3, 2019 – Leti, a research institute of CEA-Tech, and Silvaco Inc., a leading global provider of software, IP and services for designing chips and electronic systems for semiconductor companies, today announced, during the 56th Design Automation Conference (DAC) in Las Vegas, a project to estimate and model the yield of ultra-low-voltage (ULV), ultra-low-leakage (ULL) static random access memory (SRAM) used in computing applications. Accurate yield prediction in the early stage of the IC design cycle lowers manufacturing costs and improves quality.

Variability in manufacturing is highly detrimental to mass production yield of silicon chips with large memories, such as embedded caches. The Accelerated Simulation of Array for Yield Assessment (ASAYA) Project at CEA-Leti aims to validate the estimates based on electrical SPICE circuit simulations against silicon results after manufacturing. The challenge is to assess whether low failure rates (in the order of one failure in 1 billion) observed in simulation guarantee acceptable production yields for SRAMs above the MB range. In the past, such failures could be investigated successfully through classical Monte Carlo-based electrical simulation of bitcells, which allowed estimations with sufficient precision of the immunity margin against failures; or through the quasi-Monte Carlo method, which consists in evaluating the margin as a "number of sigmas," assuming its distribution follows Gauss's law. Recent (2018) publications still report these methods, showcasing that finer evaluations are difficult to work through, often using in-house software, which cannot be generalized to cover all required manufacturing process, voltage and temperature (PVT) conditions for the end-user device.

The fail-detection and yield-estimation analysis at CEA-Leti will employ Silvaco's VarMan eXtreme Memory Analysis (XMA) tool. The project will use extreme yield estimation (XYE) analysis to obtain failure rates and yield estimation at the full memory-circuit level, and extreme fail detection (XFD) analysis to investigate the PVT-dependent failure modes. VarMan employs machine-learning and flow-optimization methods to enable variability analysis of more than 6-sigma in a reasonable runtime.

"Setting up advanced methods is essential with emerging technologies developed by CEA-Leti and the increase of memories' needs. If a new method allows characterizing memory designs more quickly at a given condition of use, the entire characterization process that covers all conditions is accelerated," said Emmanuel Sabonnadiere, CEO of CEA-Leti. "We therefore have a faster method to validate our memory with confidence that it will work within the expected failure rate, which will be compatible with the cost of production and market expectations.

"For instance, the technological impact of the non-normality we have seen might lead to unexpected failures in all cases where the product operating conditions are pushed very close to the expected performance limits," he said, "in particular for memories in Internet of Things products."

The research team is analyzing a 256 Kb ULV/ULL SRAM designed by CEA-Leti. Against current assumptions used in industry about yield and variability, evidence of non-Gaussian margin distribution in some cases has been found with the help of Silvaco VarMan. The project will feature measurements of silicon dies processed in the 28nm Ultra-Thin Fully Depleted Silicon on Insulator (UT-FDSOI) technology from STMicroelectronics to assess the predictive power of VarMan XMA.

"Efficiently detecting failures and accurately estimating yield in SRAM and other kinds of memory arrays are fundamental to the development of reliable electronic devices," said Firas Mohamed, VP/GM Machine Learning & Flow Optimization Division at Silvaco. "Shrinking silicon geometries and growing complexity are placing an even greater premium on fast statistical analysis to capture and evaluate all the variability effects found in nanometer-scale design. Building on past successes of CEA-Leti and Silvaco's collaboration, this project will provide technologists with a powerful, high-accuracy predictive technology from Silvaco validated by CEA-Leti's physical silicon production. We are gratified that CEA-Leti has chosen Silvaco and its trusted high-sigma-analysis technology for this project."

About CEA-Leti

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 1,900, a portfolio of 2,700 patents, 91,500 sq. ft. of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley and Tokyo. Leti has launched 60 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in innovative R&D, defence & security, nuclear energy, technological research for industry and fundamental science, identified by Thomson Reuters as the second most innovative research organization in the world. CEA Tech leverages a unique innovation-driven culture and unrivalled expertise to develop and disseminate new technologies for industry, helping to create high-end products and provide a competitive edge.

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About Silvaco, Inc.

Silvaco Inc. is a leading EDA tools and semiconductor IP provider used for process and device development for advanced semiconductors, power IC, display and memory design. For over 30 years, Silvaco has enabled its customers to develop next generation semiconductor products in the shortest time with reduced cost. We are a technology company outpacing the EDA industry by delivering innovative smart silicon solutions to meet the world's ever-growing demand for mobile intelligent computing. The company is headquartered in Santa Clara, California and has a global presence with offices located in North America, Europe, Japan and Asia.

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